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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/681,274	10/09/2003	Yoshikazu Ohara	4074-8	5972
23117	7590	07/27/2005	EXAMINER	
NIXON & VANDERHYE, PC 901 NORTH GLEBE ROAD, 11TH FLOOR ARLINGTON, VA 22203			DICKEY, THOMAS L	
			ART UNIT	PAPER NUMBER
			2826	

DATE MAILED: 07/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/681,274

Applicant(s)

OHARA, YOSHIKAZU

Examiner

Thomas L. Dickey

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 27 June 2005.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-13 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 4-6 and 13 is/are allowed.
- 6) ☒ Claim(s) 1-3 and 7-12 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 09 October 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

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## **DETAILED ACTION**

### ***Continued Examination Under 37 CFR 1.114***

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 06/27/2005 has been entered.

### ***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3 and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by OKADA (5,531,002).

Okada discloses a semiconductor device with a flexible semiconductor chip including an element forming region 911 where a semiconductor element 955 is formed and an element non-forming region 912-913 where no semiconductor element 955 is formed, each of the element forming region 911 and the element non-forming region 912-913 be-

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ing provided on a front surface of a silicon substrate 910, a plurality of grooves (no part #, seen under a portion 912 of the element non-forming region 912-913), formed parallel to each other and having a wider width in an opening portion than in a bottom portion, formed in a portion of a rear surface of said silicon substrate 910 corresponding to said element non-forming region 912-913, wherein said groove does not extend all the way through the silicon substrate 910, so that the semiconductor chip is flexible, and wherein the groove is not provided under any portion of the element forming region 911. Note figures 40-42 and column 27 lines 11-46 of Okada.

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

A. Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over OKADA (5,531,002).

Okada discloses a semiconductor device with every limitation of claims 10 and 11 except that a material softer than the silicon substrate fills the grooves and coats the rear surface of said silicon substrate. Note figures 40-42 and column 27 lines 11-46 of Okada.

However, a second embodiment disclosed by Okada discloses a semiconductor device with silicon oil (a material softer than silicon) filling grooves 201 and coating the rear

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surface of a silicon substrate 200. Note figures 32A-C and 33 and column 25 lines 1-5 of Okada. Therefore, it would have been obvious to a person having skill in the art to augment Okada's semiconductor device with the silicon oil filling the grooves and coating the rear surface of said silicon substrate, such as taught by Okada's second embodiment in order to provide impact or vibration absorbing effect to thus provide improved impact and vibration resistance.

B. Claims 7 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over OKADA (5,531,002) in view of KNECHT ET AL. (4,905,575).

Okada discloses a semiconductor device with every limitation of claims 7 and 9 except that the groove has a substantially uniform width from a bottom portion to an opening portion of said groove, as recited in claim 7, or wherein said groove has a bottom portion with a curved surface, as recited in claim 9. Note figures 40-42 and column 27 lines 11-46 of Okada.

However, with regard to claim 7, Knecht et al. discloses a semiconductor device 70 having an element forming region 71 where a semiconductor element is formed and an element non-forming region 76 where no semiconductor element is formed, on a front surface of a silicon substrate 72, comprising a plurality of grooves 75 each having substantially uniform width from a bottom portion to an opening portion of that groove 75. Note figure 6 of Knecht et al. Further, with regard to claim 9, Knecht et al. discloses a semiconductor device 90 having an element forming region 94 where a semiconductor element 91 is formed and an element non-forming region 97 where no semiconductor element

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formed, on a front surface of a silicon substrate 92, comprising a plurality of grooves 95 having bottom portions with curved surfaces. Note figure 8 of Knecht et al. Therefore, it would have been obvious to a person having skill in the art to augment of Okada's semiconductor device with the groove having a substantially uniform width from a bottom portion to an opening portion of said groove, or the groove having a bottom portion with a curved surface, such as taught by Knecht et al. in order to provide a different clearance between parts of the silicon substrate to thus optimize flexibility according to need.

C. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over OKADA (5,531,002) in view of WILLIS ET AL. (5,912,427).

Okada discloses a semiconductor device with every limitation of claim 12 except that a plurality of said element forming regions are isolated from each other, and said element non-forming region is a region sandwiched between said element forming regions. Note figures 40-42 and column 27 lines 11-46 of Okada.

However, Willis et al. discloses a semiconductor device 500 having silicon substrate 501 coating the rear surface of said silicon substrate 501; a plurality of element forming regions 580 isolated from each other, where semiconductor elements are formed; and an element non-forming region 510, sandwiched between said element forming regions 580, where a semiconductor element is not formed, on a front surface of said silicon substrate 501, said semiconductor device 500 comprising a groove 503 formed in a portion of a rear surface of said substrate 501 corresponding to said element non-forming region 510. Note figure 12 and column 9 lines 1-15 of Willis et al. Therefore, it would have been obvious to

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a person having skill in the art to augment of Okada's semiconductor device with the plurality of said element forming regions, isolated from each other, wherein said element non-forming region is a region sandwiched between said element forming regions, such as taught by Willis et al. in order to increase the number of element forming region and thus the number of elements, to thus provide increased functionality.

### ***Response to Arguments***

Applicant's argument with respect to claim 1 has been considered but is moot in view of the new ground(s) of rejection.

### ***Allowable Subject Matter***

4. Claims 4-6 and 13 are allowable are allowed over the references of record because none of these references disclosed or can be combined to yield the claimed invention such as a semiconductor device having an element forming region where a semiconductor element is formed and an element non-forming region where a semiconductor element is not formed, on a front surface of a silicon substrate, comprising a groove formed in a portion of a rear surface of said substrate corresponding to said element non-forming region, wherein said grooves are formed to extend in directions crossing each other, as recited in claim 4, or said semiconductor device, bonded to a **curved** bonding substrate, as recited in claim 13.

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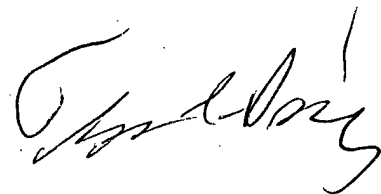
**Conclusion**

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913.

The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



**Thomas L. Dickey**  
**Patent Examiner**  
**Art Unit 2826**  
**12/04**